

Team 2: ATC Lite Product Verification

Katherine Abernathy, Andrew Hoover, Jaime Malone,





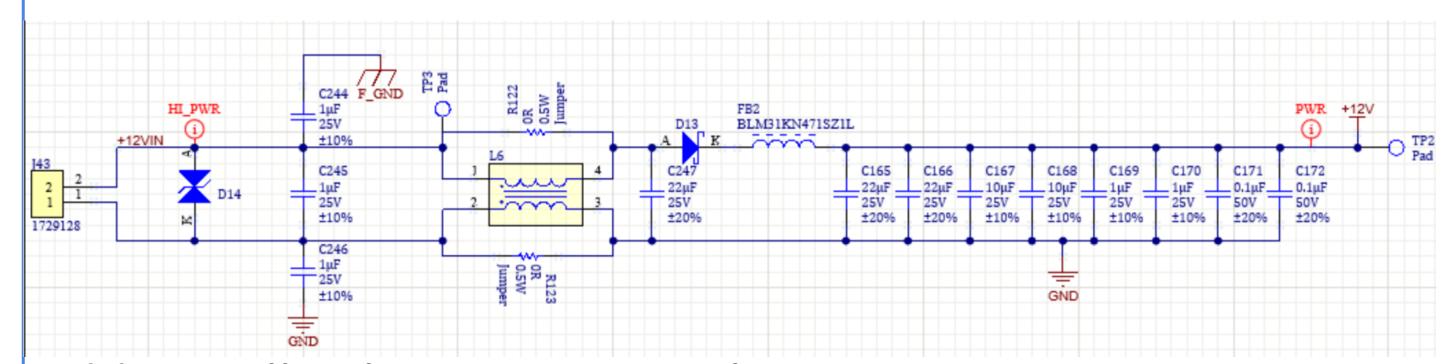
Executive Summary

The purpose of this project was to investigate, debug, and develop a comprehensive test plan for the electronic hardware and firmware of the ATC Lite. This included completing a discovery phase, presenting proposed tests and testing methods, assessing and debugging the hardware for functionality, evaluating firmware, and developing remaining features while integrating hardware and software. Additionally, the project aimed to evaluate thermal, shock, and vibration limits through mechanical engineering assessment.

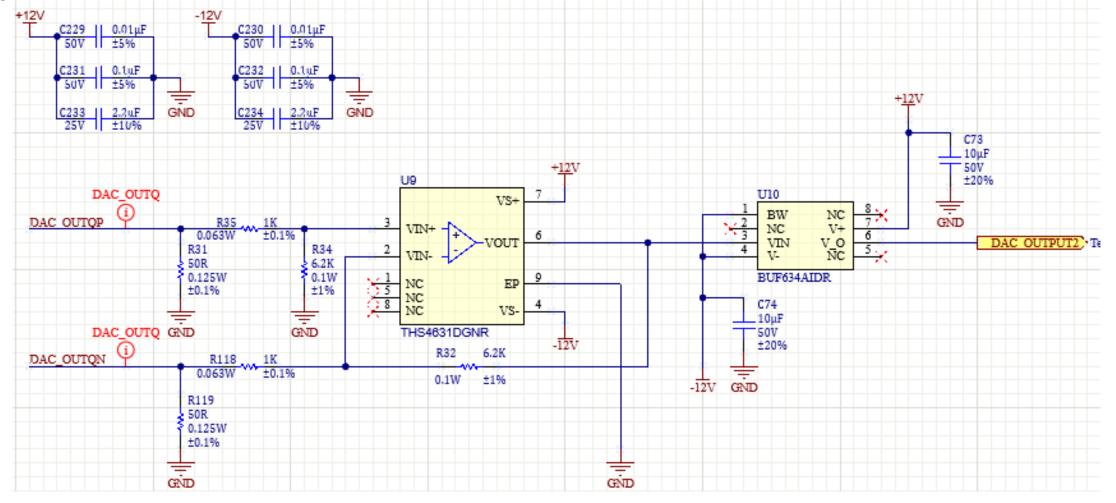


Schematic Changes

A new revision of the PCB was created and adjustments were made to existing circuits to decrease noise and decrease the product's susceptibility to electromagnetic emissions.

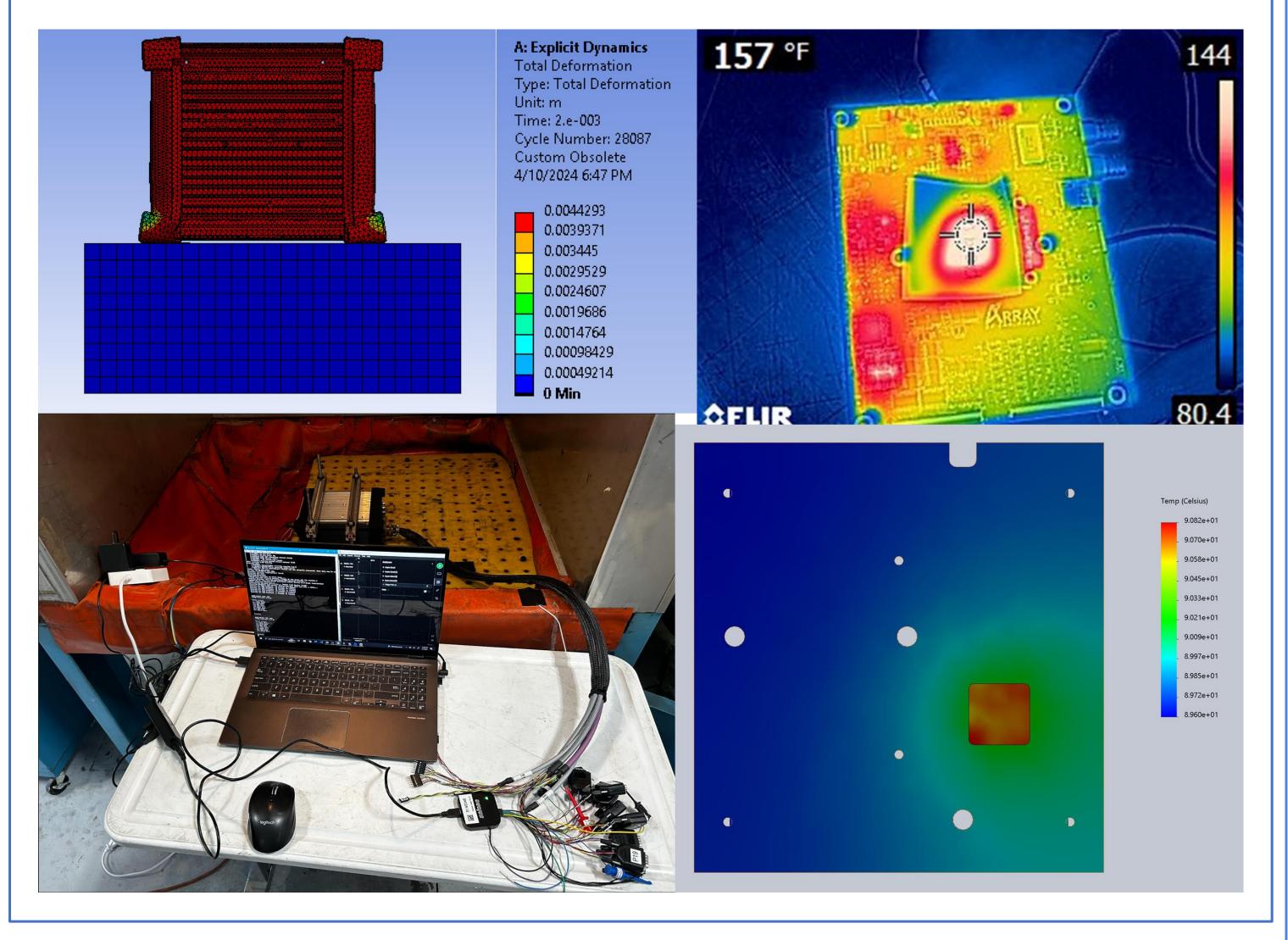


Additionally, the DAC circuit that was incorrect in revision 1 was updated and verified.



Mechanical Testing

Simulations were run for thermal testing and shock testing. Vibration, thermal and shock testing were also physically conducted to ISO 16750-3 standard.



Notable Challenges

- One working development board at the beginning of the project created hesitation towards modifying the board.
- Testing had the possibility of being destructive, so it had to be done at the end of the project timeline.
- Paywall for standards made it difficult to select a testing standard before purchasing.

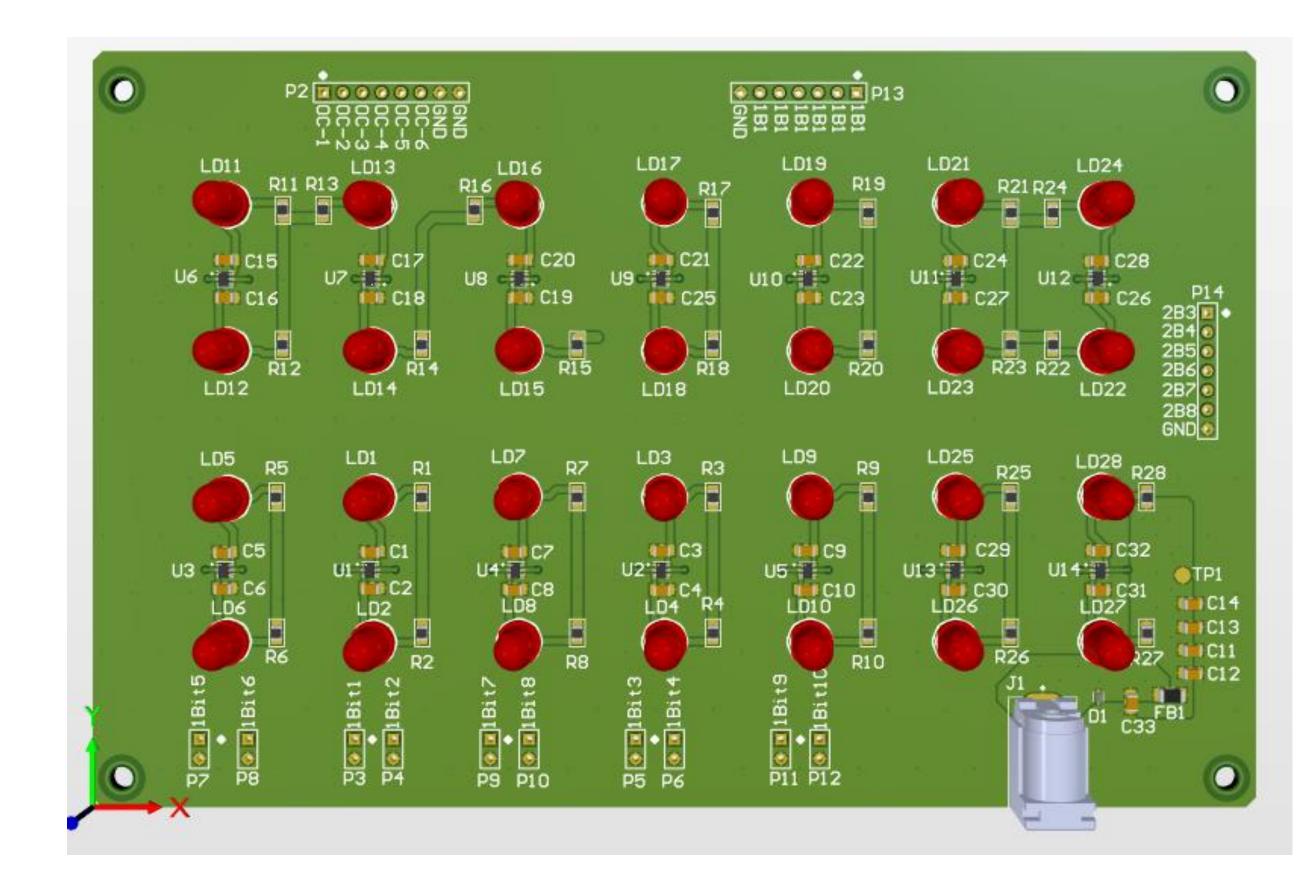
Achievements

- The SD card circuit was debugged and hand modified.
- A working DAC circuit was developed and verified.
 - All IP Core functionality was confirmed.
 - The ATC Lite passed all mechanical tests.
 - A test plan and datasheet for the ATC Lite were developed.

Special thanks to Dr. Brakora and Dr. Krug for their support and recommendations and to Array of Engineers for sponsoring our project!

Electrical and Logical Testing

The focus of this project iteration was to provide all the necessary information and hardware to conduct verification testing of the product. This included the development of a GPIO load box for monitoring the GPIO signals external to the unit itself during EMC/EMI testing. The PCB that was developed as part of this load box is shown below.



Integration testing of all the firmware was also completed. Each of the IP cores was tested indirectly using system tests. To do this, a baremetal environment was set up and a test program was written to give the tester the ability to select an IP core and specific functionality to test through serial communication with the ATC Lite.

